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Whereas the Parliament of India has set out to provide a practical regime of right to information for citizens to secure access to information under the control of public authorities, in order to promote transparency and accountability in the working of every public authority, and whereas the attached publication of the Bureau of Indian Standards is of particular interest to the public, particularly disadvantaged communities and those engaged in the pursuit of education and knowledge, the attached public safety standard is made available to promote the timely dissemination of this information in an accurate manner to the public.

“जानने का अधिकार, जीने का अधिकार”
Satyanarayan Gangaram Pitroda
“The Right to Information, The Right to Live”

“पुराने को छोड़ नये के तरफ”
Jawaharlal Nehru
“Step Out From the Old to the New”

Indian Standard

SEMICONDUCTOR DEVICES — DISCRETE DEVICES AND INTEGRATED CIRCUITS

PART 8 FIELD-EFFECT TRANSISTORS

( First Revision )

ICS 31.080.30
NATIONAL FOREWORD

This Indian Standard (Part 8) (First Revision) which is identical with IEC 60747-8 : 2000 ‘Semiconductor devices — Part 8: Field-effect transistors’ issued by the International Electrotechnical Commission (IEC) was adopted by the Bureau of Indian Standards on the recommendation of the Semiconductor and Other Electronic Components and Devices Sectional Committee and approval of the Electronics and Information Technology Division Council.

This standard was originally published in 2001 and was based on IEC 60747-8 : 1984 and has now been revised to align it with the latest IEC Publication.

The text of the IEC Standard has been approved as suitable for publication as an Indian Standard without deviations. Certain conventions are, however, not identical to those used in Indian Standards. Attention is particularly drawn to the following:

a) Wherever the words ‘International Standard’ appear referring to this standard, they should be read as ‘Indian Standard’.

b) Comma (,) has been used as a decimal marker in the International Standards while in Indian Standards, the current practice is to use a point (.) as the decimal marker.

In this adopted standard, reference appears to certain International Standards for which Indian Standards also exist. The corresponding Indian Standards which are to be substituted in their respective places are listed below along with their degree of equivalence for the editions indicated:

<table>
<thead>
<tr>
<th>International Standard</th>
<th>Corresponding Indian Standard</th>
<th>Degree of Equivalence</th>
</tr>
</thead>
</table>

Only the English language text in the International Standard has been retained while adopting it in this Indian Standard, and as such the page numbers given here are not the same as in the IEC Standard.

For the purpose of deciding whether a particular requirement of this standard is complied with, the final value, observed or calculated, expressing the result of a test or analysis, shall be rounded off in accordance with IS 2 : 1960 ‘Rules for rounding off numerical values (revised)’. The number of significant places retained in the rounded off value should be the same as that of the specified value in this standard.

Since revised in 2006.
1 Scope

This part of IEC 60747 gives standards for the following categories of field-effect transistors:

- type A: junction-gate type;
- type B: insulated-gate depletion type;
- type C: insulated-gate enhancement type.

2 Normative references

The following normative documents contain provisions which, through reference in this text, constitute provisions of this part of IEC 60747. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this part of IEC 60747 are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references, the latest edition of the normative document referred to applies. Members of IEC and ISO maintain registers of currently valid International Standards.


IEC 60747-7:2000, Semiconductor devices – Part 7: Bipolar transistors
3 Classification

Since a field-effect transistor may have one or several gates, the following classification results:

```
Field-effect devices
(a source, a drain, one or several gates)
```

- Devices with one or several P channels
  - Junction-gate devices
  - Schottky barrier-gate devices
  - Insulated-gate devices
  - MESFET
  - MODFET
  - HEMT

- Devices with one or several N channels
  - Junction-gate devices
  - Schottky barrier-gate devices
  - Insulated-gate devices
  - MOSFET
  - MODFET
  - Other insulated-gate FET

**NOTE** Schottky barrier-gate and insulated gate devices have depletion type devices and enhancement type devices.

4 Terminology and letter symbols

For the purpose of this part of IEC 60747, the following definitions and symbols apply:

4.1 Types of field-effect transistors

4.1.1 N-channel field-effect transistor
a field-effect transistor that has one or more N-type conduction channels

4.1.2 P-channel field-effect transistor
a field-effect transistor that has one or more P-type conduction channels

4.1.3 junction-gate field-effect transistor (JFET)
a field-effect transistor in which:
- the source and drain regions are connected with each other by the channel region, all three being of the same conductivity type;
- a gate region adjacent to the channel has the opposite conductivity type, thus forming with source, channel and drain region a PN junction, and
- the gate-source voltage controls the conductivity of the conduction channel in the channel region by controlling the width of the gate space-charge region and hence also the remaining cross-section of the conduction channel
4.1.4 Insulated-gate field-effect transistor (IGFET)
a field-effect transistor in which:
- one or more gate electrodes are electrically insulated from the body;
- the conductivity type of both the source and drain regions is opposite from that of the semiconductor body in which they are located;
- the principal current flows in a channel that is formed by an inversion layer connecting source and drain regions;
- the inversion layer is either already present at zero gate-source voltage or produced within the body at sufficiently high forward gate-source voltage by accumulation of the minority charge carriers of the body material, and
- the conductance of the channel is controlled by the gate-source voltage, which controls the electric field between gate electrode and the body and hence the amount of accumulated minority charge carriers.

4.1.5 Metal-oxide-semiconductor field-effect transistor (MOSFET)
an insulated-gate field-effect transistor in which the insulating layer between each gate electrode and the channel is oxide material.

4.1.6 Depletion-type field-effect transistor
a field-effect transistor in which an inversion layer present at the surface of the active semiconductor region causes an appreciable channel conductance that may be increased (decreased) by applying a forward (reverse) gate-source voltage.

4.1.7 Enhancement-type field-effect transistor
a field-effect transistor having substantially zero channel conductance at zero gate-source voltage, and in which a conduction channel may be obtained by applying a sufficiently high forward gate-source voltage, which induces an inversion layer below the gate electrode.

4.1.8 Single-gate field-effect transistor
a field-effect transistor having a gate region, a source region, and a drain region.

NOTE The term may be abbreviated to "field-effect transistor", if no ambiguity is likely to occur.

4.1.9 Dual-gate field-effect transistor
a field-effect transistor having two independent gate regions, a source region, and a drain region.

4.1.10 Schottky-barrier-gate field-effect transistor
a field-effect transistor in which:
- the source and drain regions are connected with each other by the channel region, all three being of the same conductivity type;
- one or more gate electrodes each form a Schottky-barrier with the channel region;
- the gate-source voltage controls the conductance of the conduction channel by varying its cross-section.
4.1.11 metal-semiconductor field-effect transistor (MESFET)
a Schottky-barrier-gate field-effect transistor in which the gate electrodes are metal

4.1.12 modulation-doped field-effect transistor (MODFET) or high electron mobility transistor (HEMT)
a metal-semiconductor field-effect transistor in which a doped material forms a heterojunction with an undoped channel; the doped material supplies electrons to the undoped channel whose high electron mobility results in enhanced channel conductance
NOTE MODFET and HEMT may be used interchangeably.

4.2 General terms

4.2.1 Physical region (of a field-effect transistor)

4.2.1.1 source region (of a field-effect transistor)
the physical region that is designed by the manufacturer to contain the supply region under the defined operating conditions to which the specifications refer

4.2.1.2 drain region (of a field-effect transistor)
the physical region that is designed by the manufacturer to contain the collection region under the defined operating conditions to which the specifications refer

4.2.1.3 gate region of an IGFET
the insulating layer between the gate electrode and the surface of the semiconductor body, below which the channel is or may be formed

4.2.1.4 gate region of an JFET
the region below the gate electrode that is of opposite conductivity type from that of the source, channel and drain regions

4.2.1.5 channel region of a depletion-type IGFET
the inversion layer technologically placed below the gate region

4.2.1.6 channel region of a JFET
the region between source region and drain region that has the same conductivity type as these two regions

4.2.1.7 subchannel region of an IGFET
the region between source region and drain region, excluding the channel region of a depletion-type IGFET and all pertinent transition zones
4.2.1.8 substrate (of a JFET or IGFET)
1) the part of the original material that remains unchanged when the device elements are formed upon or within the original material
   NOTE The original material may be a layer of semiconductor material cut from a single crystal, a layer of semiconductor material deposited on a supporting base, or the supporting base itself.
2) the original semiconductor material before being processed
   NOTE The intended meaning will become clear from the context in which the term is used. If necessary, distinction could be made between the “original substrate” and the “remaining substrate”.

4.2.1.9 substrate (of a thin film field effect transistor)
an insulator that supports the source and drain electrodes, the insulating gate layer, and the thin semiconductor layer

4.2.2 Functional regions

4.2.2.1 functional source region
a supply region that delivers principal-current charge carriers into the channel

4.2.2.2 functional drain region
a collection region that acquires principal-current charge carriers from the channel

4.2.2.3 channel of a IGFET
the functional region through which the principal-current charge carriers pass and in which the carrier concentration is determined by the gate-source voltage, the principal current being the result of the drift field produced by the drain-source voltage

4.2.2.4 channel of a JFET
the functional region through which the principal-current charge carriers pass and whose cross-section is determined by the applied gate-source voltage, the principal current being the result of the drift field produced by the drain-source voltage

4.2.2.5 subchannel space-charge region of an IGFET
the space-charge region associated with the transition regions between the subchannel region on one side, and source region, channel region and drain region on the other side

4.2.2.6 functional subchannel region
the remaining neutral part of the (physical) subchannel region that is confined by the surrounding subchannel space-charge region
4.3 Terms related to ratings and characteristics

NOTE When several distinctive forms of a letter symbol exist, the most commonly used form is given.

4.3.1 "reverse" and "forward" directions
here "reverse" means: the direction in which the channel carriers are decreased (depleted), and "forward" means: the direction in which the channel carriers are increased (enhanced)

4.3.2 threshold voltage (of an enhancement type field-effect transistor) \( V_{GS(TO)} \)
the gate-source voltage at which the magnitude of the drain current reaches a specified low value

4.3.3 cut-off voltage (of a depletion type field-effect transistor) \( V_{GS(off)} \)
the gate-source voltage at which the magnitude of the drain current reaches a specified low value

4.3.4 gate cut-off current (of a junction-gate field-effect transistor)
the current flowing in the gate terminal of a junction field-effect transistor when the gate junction is biased in the reverse direction

4.3.5 gate leakage current (of an insulated-gate field-effect transistor)
the leakage current flowing in the gate terminal of an insulated-gate field-effect transistor

4.3.6 Capacitances

4.3.6.1 (short-circuit) Input capacitance \( C_{iss} \)
the capacitance between the gate and source terminals with the drain terminal short-circuited to the source terminal for a.c. signals

4.3.6.2 (short-circuit) output capacitance \( C_{oss} \)
the capacitance between the drain and source terminals with the gate terminal short-circuited to the source terminal for a.c. signals

4.3.6.3 (short-circuit) reverse transfer capacitance \( C_{rss} \)
the capacitance between the drain and gate terminals with the source terminal short-circuited to the gate terminal for a.c. signals

4.3.7 gate-source resistance \( r_{GS} \)
the d.c. resistance between gate and source terminals at specified gate-source and drain-source voltages

4.3.8 drain-source on-state resistance \( r_{Dson} \)
the d.c. resistance between the drain and source terminals when the FET is in its on-state
4.3.9  
gate charge $Q_{gs}$  
the charge required to raise the gate-source voltage from zero to a specified value  

4.4  Letter symbols  

4.4.1  General  
Clauses 2, 3 and 4, chapter V of IEC 60747-1 apply.  

4.4.2  Additional general subscripts  
In addition to the list of recommended general subscripts given in 2.2.1, chapter V of IEC 60747-1, the following special subscripts are recommended for field-effect transistors:  

D, d = drain  
G, g = gate  
S, s = source  
B, b; U, u = substrate  
T; th; (TO) = threshold  

4.4.3  List of letter symbols  

<table>
<thead>
<tr>
<th>Name and designation</th>
<th>Letter symbol</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.4.3.1 Voltage</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Drain-source (d.c.) voltage</td>
<td>$V_{DS}$</td>
<td></td>
</tr>
<tr>
<td>Gate-source (d.c.) voltage</td>
<td>$V_{GS}$</td>
<td></td>
</tr>
<tr>
<td>Gate-source cut-off voltage (of a junction field-effect transistor and of a depletion type insulated-gate field-effect transistor)</td>
<td>$V_{GS(Off)}$; $V_{GS(max)}$</td>
<td></td>
</tr>
<tr>
<td>Gate-source threshold voltage (of an enhancement type insulated-gate field-effect transistor)</td>
<td>$V_{GST}$; $V_{GS(pk)}$; $V_{GS(TO)}$</td>
<td></td>
</tr>
<tr>
<td>Forward gate-source (d.c.) voltage</td>
<td>$V_{GSSF}$</td>
<td></td>
</tr>
<tr>
<td>Reverse gate-source (d.c.) voltage</td>
<td>$V_{GSR}$</td>
<td></td>
</tr>
<tr>
<td>Gate-drain (d.c.) voltage</td>
<td>$V_{GD}$</td>
<td></td>
</tr>
<tr>
<td>Source-substrate (d.c.) voltage</td>
<td>$V_{SB}$; $V_{SU}$</td>
<td></td>
</tr>
<tr>
<td>Drain-substrate (d.c.) voltage</td>
<td>$V_{DB}$; $V_{DU}$</td>
<td></td>
</tr>
<tr>
<td>Gate-substrate (d.c.) voltage</td>
<td>$V_{GS1}$; $V_{GSU}$</td>
<td></td>
</tr>
<tr>
<td>Gate-gate voltage (for multi-gate devices)</td>
<td>$V_{GT-G2}$</td>
<td></td>
</tr>
<tr>
<td>Gate-source breakdown voltage with drain short-circuited to source</td>
<td>$V_{BRIGSS}$</td>
<td></td>
</tr>
</tbody>
</table>
### 4.4.3.2 Currents

<table>
<thead>
<tr>
<th>Name and designation</th>
<th>Letter symbol</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain (d.c.) current</td>
<td>$I_D$</td>
<td></td>
</tr>
<tr>
<td>Drain current, at a specified gate-source condition</td>
<td>$I_{DSX}$</td>
<td></td>
</tr>
<tr>
<td>Drain current, at a specified external gate-source resistance</td>
<td>$I_{GSR}$</td>
<td></td>
</tr>
<tr>
<td>Drain current, with gate short-circuited to source ($V_{GS} = 0$)</td>
<td>$I_{DSS}$</td>
<td></td>
</tr>
<tr>
<td>Source (d.c.) current</td>
<td>$I_S$</td>
<td></td>
</tr>
<tr>
<td>Source current, at a specified gate-drain condition</td>
<td>$I_{SDX}$</td>
<td></td>
</tr>
<tr>
<td>Source current, with gate short-circuited to drain ($V_{GD} = 0$)</td>
<td>$I_{SDS}$</td>
<td></td>
</tr>
<tr>
<td>Gate (d.c.) current</td>
<td>$I_G$</td>
<td></td>
</tr>
<tr>
<td>Forward gate current</td>
<td>$I_{GF}$</td>
<td></td>
</tr>
<tr>
<td>Gate cut-off current (of a junction field-effect transistor), with source open-circuited</td>
<td>$I_{DSD}$</td>
<td></td>
</tr>
<tr>
<td>Gate-cut-off current (of a junction field-effect transistor), with drain open-circuited</td>
<td>$I_{GSO}$</td>
<td></td>
</tr>
<tr>
<td>Gate cut-off current (of a junction field-effect transistor), with drain short-circuited to source</td>
<td>$I_{GSS}$</td>
<td></td>
</tr>
<tr>
<td>Gate leakage current (of an insulated-gate field-effect transistor), with drain short-circuited to source</td>
<td>$I_{GSS}$</td>
<td></td>
</tr>
<tr>
<td>Gate cut-off current (of a junction field-effect transistor), with specified drain-source circuit conditions</td>
<td>$I_{GSSX}$</td>
<td></td>
</tr>
<tr>
<td>Substrate current</td>
<td>$I_S; I_U$</td>
<td></td>
</tr>
</tbody>
</table>

### 4.4.3.3 Power dissipation

<table>
<thead>
<tr>
<th>Name and designation</th>
<th>Letter symbol</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain-source (d.c.) power dissipation</td>
<td>$P_{DS}$</td>
<td></td>
</tr>
<tr>
<td>Name and designation</td>
<td>Letter symbol</td>
<td>Remarks</td>
</tr>
<tr>
<td>----------------------</td>
<td>--------------</td>
<td>---------</td>
</tr>
<tr>
<td>Drain-source resistance</td>
<td>$r_{ds}$</td>
<td></td>
</tr>
<tr>
<td>Gate-source resistance</td>
<td>$r_{gs}$</td>
<td></td>
</tr>
<tr>
<td>Gate-drain resistance</td>
<td>$r_{gd}$</td>
<td></td>
</tr>
<tr>
<td>Gate resistance (with $V_{DS} = 0$ or $V_{GS} = 0$)</td>
<td>$r_{GSS}$</td>
<td></td>
</tr>
<tr>
<td>Drain-source on-state resistance</td>
<td>$r_{DS(ON)}$</td>
<td></td>
</tr>
<tr>
<td>Drain-source off-state resistance</td>
<td>$r_{DS(OFF)}$</td>
<td></td>
</tr>
<tr>
<td>Open-circuit gate-source capacitance (drain-source and gate-drain open-circuited to a.c.)</td>
<td>$C_{geo}$</td>
<td></td>
</tr>
<tr>
<td>Open-circuit gate-drain capacitance (drain-source and gate-source open-circuited to a.c.)</td>
<td>$C_{gdo}$</td>
<td></td>
</tr>
<tr>
<td>Open-circuit drain-source capacitance (gate-drain and gate-source open-circuited to a.c.)</td>
<td>$C_{eso}$</td>
<td></td>
</tr>
<tr>
<td>Short-circuit input capacitance in common-source configuration; gate-source capacitance (drain-source short-circuited to a.c.)</td>
<td>$C_{ias}; C_{1ias}$</td>
<td></td>
</tr>
<tr>
<td>Short-circuit output capacitance in common-source configuration; drain-source capacitance (gate-source short-circuited to a.c.)</td>
<td>$C_{oes}; C_{22as}$</td>
<td></td>
</tr>
<tr>
<td>Short-circuit input conductance in common-source configuration</td>
<td>$G_{ias}$</td>
<td></td>
</tr>
<tr>
<td>Short-circuit output conductance in common-source configuration</td>
<td>$G_{oes}$</td>
<td></td>
</tr>
<tr>
<td>Common-source reverse transfer capacitance with input short-circuited to a.c.</td>
<td>$C_{res}; C_{i12as}$</td>
<td></td>
</tr>
<tr>
<td>Short-circuit output capacitance in common-drain configuration (gate-drain short-circuited to a.c.)</td>
<td>$C_{ode}; C_{22ds}$</td>
<td></td>
</tr>
<tr>
<td>Name and designation</td>
<td>Letter symbol</td>
<td>Remarks</td>
</tr>
<tr>
<td>----------------------</td>
<td>--------------</td>
<td>---------</td>
</tr>
<tr>
<td>4.4.3.5 Small-signal parameters (see figures 1, 2 and 3)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
| Short-circuit input admittance | \( y_{Is} = \Re(y_{Is}) + j\omega C_{Is} \)  
\( y_{1Is} = \Re(y_{11s}) + j\omega C_{11s} \) | |
| Short-circuit reverse transfer admittance | \( y_{Rs} = \Re(y_{Rs}) + j\omega C_{Rs} \)  
\( y_{12s} = \Re(y_{12s}) + j\omega C_{12s} \) | |
| Short-circuit forward transfer admittance | \( y_{Fs} = \Re(y_{Fs}) + j\omega C_{Fs} \)  
\( y_{21s} = \Re(y_{21s}) + j\omega C_{21s} \) | |
| Short-circuit output admittance | \( y_{os} = \Re(y_{os}) + j\omega C_{os} \)  
\( y_{22s} = \Re(y_{22s}) + j\omega C_{22s} \) | |
| Modulus of the short-circuit reverse transfer admittance | \( |y_{Rs}| \) \(|y_{12s}| \) | |
| Phase of the short-circuit reverse transfer admittance | \( \phi_{yRs} \) \( \phi_{y12s} \) | |
| Modulus of the short-circuit forward transfer admittance | \( |y_{Fs}| \) \(|y_{21s}| \) | |
| Phase of the short-circuit forward transfer admittance | \( \phi_{yFs} \) \( \phi_{y21s} \) | |
| Gate-source conductance (in the \( \pi \) equivalent circuit) | \( g_{gs} \) | |
| Gate-drain conductance (in the \( \pi \) equivalent circuit) | \( g_{gd} \) | |
| Drain-source conductance (in the \( \pi \) equivalent circuit) | \( g_{ds} \) | |
| Forward transconductance (in the \( \pi \) equivalent circuit) | \( g_{ms} \) \( g_{m} \) | |
| Gate-source capacitance (in the \( \pi \) equivalent circuit) | \( C_{gs} \) | |
| Gate-drain capacitance (in the \( \pi \) equivalent circuit) | \( C_{gd} \) | |
| Drain-source capacitance (in the \( \pi \) equivalent circuit) | \( C_{ds} \) | |
## 4.4.3.5 Small-signal parameters (continued)

<table>
<thead>
<tr>
<th>Name and designation</th>
<th>Letter symbol</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input reflection coefficient:</td>
<td>$s_{11s}$ or $s_{11g}$</td>
<td></td>
</tr>
<tr>
<td>- in common-source configuration</td>
<td></td>
<td></td>
</tr>
<tr>
<td>- in common-gate configuration</td>
<td>$s_{11g}$ or $s_{11d}$</td>
<td></td>
</tr>
<tr>
<td>- in common-drain configuration</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output reflection coefficient:</td>
<td>$s_{22s}$ or $s_{22g}$</td>
<td></td>
</tr>
<tr>
<td>- in common-source configuration</td>
<td></td>
<td></td>
</tr>
<tr>
<td>- in common-gate configuration</td>
<td>$s_{22g}$ or $s_{22d}$</td>
<td></td>
</tr>
<tr>
<td>- in common-drain configuration</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Forward transmission coefficient:</td>
<td>$s_{21s}$ or $s_{21g}$</td>
<td></td>
</tr>
<tr>
<td>- in common-source configuration</td>
<td></td>
<td></td>
</tr>
<tr>
<td>- in common-gate configuration</td>
<td>$s_{21g}$ or $s_{21d}$</td>
<td></td>
</tr>
<tr>
<td>- in common-drain configuration</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reverse transmission coefficient:</td>
<td>$s_{12s}$ or $s_{12g}$</td>
<td></td>
</tr>
<tr>
<td>- in common-source configuration</td>
<td></td>
<td></td>
</tr>
<tr>
<td>- in common-gate configuration</td>
<td>$s_{12g}$ or $s_{12d}$</td>
<td></td>
</tr>
<tr>
<td>- in common-drain configuration</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

## 4.4.3.6 Other parameters

<table>
<thead>
<tr>
<th>Name and designation</th>
<th>Letter symbol</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power gain</td>
<td>$G_p$</td>
<td></td>
</tr>
<tr>
<td>Cut-off frequency (in the common-source configuration)</td>
<td>$f_{Tss}$</td>
<td></td>
</tr>
<tr>
<td>Noise voltage</td>
<td>$V_n$</td>
<td></td>
</tr>
<tr>
<td>Noise figure</td>
<td>$F$</td>
<td></td>
</tr>
<tr>
<td>Temperature coefficient of drain current</td>
<td>$a_D$</td>
<td></td>
</tr>
<tr>
<td>Temperature coefficient of drain-source resistance</td>
<td>$a_{ds}$</td>
<td></td>
</tr>
<tr>
<td>Turn-on delay time</td>
<td>$t_{(on)}$</td>
<td></td>
</tr>
<tr>
<td>Turn-off delay time</td>
<td>$t_{(off)}$</td>
<td></td>
</tr>
<tr>
<td>Rise time</td>
<td>$t_r$</td>
<td></td>
</tr>
<tr>
<td>Fall time</td>
<td>$t_f$</td>
<td></td>
</tr>
<tr>
<td>Turn-on time</td>
<td>$t_{on}$</td>
<td></td>
</tr>
<tr>
<td>Turn-off time</td>
<td>$t_{off}$</td>
<td></td>
</tr>
<tr>
<td>Switching times (see figure 4)</td>
<td>$t_{on} = t_{(on)} + t_r$</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$t_{off} = t_{(off)} + t_f$</td>
<td></td>
</tr>
<tr>
<td>Frequency of unity forward transmission coefficient:</td>
<td>$f_{ss}$ or $f_{ss}$</td>
<td></td>
</tr>
<tr>
<td>- in common-source configuration</td>
<td>$f_{ss} = f$ for $</td>
<td>s_{21s}</td>
</tr>
<tr>
<td>- in common-gate configuration</td>
<td>$f_{sg} = f$ for $</td>
<td>s_{21g}</td>
</tr>
<tr>
<td>- in common-drain configuration</td>
<td>$f_{sd} = f$ for $</td>
<td>s_{21d}</td>
</tr>
</tbody>
</table>
Figure 1

Figure 2

Figure 3

Small-signal $y$ parameters in common-source configuration and $x$ equivalent circuit parameters
4.4.3.7 Matched-pair field-effect transistors

<table>
<thead>
<tr>
<th>Name and designation</th>
<th>Letter symbol</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Difference of gate leakage currents (for insulated-gate</td>
<td>( I_{G1} - I_{G2} )</td>
<td>The smaller value is subtracted from the larger value</td>
</tr>
<tr>
<td>field-effect transistors) and difference of gate cut-off</td>
<td>( I_{GSS1} / I_{GSS2} )</td>
<td>The smaller of the two values is taken as the numerator</td>
</tr>
<tr>
<td>currents (for junction field-effect transistors)</td>
<td>( G_{os1} - G_{os2} )</td>
<td>The smaller value is subtracted from the larger value</td>
</tr>
<tr>
<td>Ratio of drain currents for zero gate-source voltage</td>
<td>( G_{os1} / G_{os2} )</td>
<td>The smaller of the two values is taken as the numerator</td>
</tr>
<tr>
<td>Difference of small-signal common-source output</td>
<td>( V_{GS1} - V_{GS2} )</td>
<td>The smaller value is subtracted from the larger value</td>
</tr>
<tr>
<td>conductances</td>
<td>(</td>
<td>\Delta(V_{GS1} - V_{GS2})</td>
</tr>
<tr>
<td>Ratio of small-signal common-source forward transfer</td>
<td>( G_{fs1} / G_{fs2} )</td>
<td></td>
</tr>
<tr>
<td>conductances</td>
<td>(</td>
<td>\Delta(V_{GS1} - V_{GS2})</td>
</tr>
<tr>
<td>Difference of gate-source voltages</td>
<td>(</td>
<td>\Delta(V_{GS1} - V_{GS2})</td>
</tr>
<tr>
<td>Change in difference of gate-source voltages between</td>
<td>(</td>
<td>\Delta(V_{GS1} - V_{GS2})</td>
</tr>
<tr>
<td>two temperatures</td>
<td>(</td>
<td>\Delta(V_{GS1} - V_{GS2})</td>
</tr>
</tbody>
</table>

Figure 4 – Switching times
5 Essential ratings and characteristics

5.1 General

5.1.1 Device categories

Field-effect transistors are divided into three categories:

- type A: junction-gate type;
- type B: insulated-gate depletion type;
- type C: insulated-gate enhancement type.

5.1.2 Multiple-gate devices

For multiple-gate devices, the required gate ratings and characteristics shall be given for each gate separately, except where otherwise stated.

5.1.3 Handling precautions

Because of the very high input resistance of field-effect transistors, the gate insulation layer (for insulated-gate types) or the gate junction (for junction-gate types) may be irreversibly damaged if an excessive voltage is allowed to build up, e.g. due to contact with electrostatically charged persons, leakage currents from soldering irons, etc.

When handling these devices, the handling precautions given in clause 1, chapter IX, of IEC 60747-1 shall therefore be observed.

5.2 Ratings (limiting values)

5.2.1 Temperatures

5.2.1.1 Minimum and maximum storage temperatures \( (T_{stg}) \)

5.2.1.2 Minimum and maximum operating temperature (ambient or case) \( (T_{amb} \text{ or } T_{case}) \)

5.2.1.3 Virtual junction temperature \( (T_{VJ}) \) (where appropriate)

Maximum rated value.

5.2.2 Power dissipation \( (P_{tot}) \)

5.2.2.1 Maximum total power dissipation \( (P_{tot max}) \) over the specified range of operating temperatures (ambient or case). Any special requirements for ventilation and/or mounting shall be stated.
Either:

5.2.2.1 A curve showing $P_{\text{tot max}}$ as a function of operating temperature ($T_{\text{amb}}$ or $T_{\text{case}}$), or (for power MOSFET only):

5.2.2.1.1 A curve showing $P_{\text{tot max}}$ as a function of operating temperature ($T_{\text{amb}}$ or $T_{\text{case}}$), or (for power MOSFET only):

5.2.2.1.2 a) Maximum virtual channel temperature ($T_{V_{\text{Y max}}}$), and

5.2.2.1.2 b) Absolute limiting value of total power dissipation ($P_{\text{tot abs}}$).

NOTE When $T_{V_{\text{Y max}}}$ and $P_{\text{tot abs}}$ are specified $R_{\text{th}}$ and, where appropriate, $Z_{\text{th}}$ should also be specified (see the relevant subclauses in 5.3).

5.2.2.2 For power MOSFET only:

Maximum peak total power dissipation ($P_{\text{tot M max}}$).

A curve, showing $P_{\text{tot M max}}$ (where appropriate).

5.2.2.3 For power MOSFET only:

Safe operating area (SOAR) where appropriate, over the specified range of operating temperatures, under specified pulse conditions.

5.2.3 Voltages and currents

Rating shall be given preferably by a curve over the range of operating temperatures, or at 25 °C and one other higher operating temperature, chosen from the list in clause 5, chapter IV of IEC 60747-1.

5.2.3.1 Maximum drain-source voltage, under specified conditions.

5.2.3.2 Maximum reverse gate-source voltage and, where appropriate, maximum forward gate-source voltage, under specified conditions.

5.2.3.3 Maximum gate-drain voltage, under specified conditions.

5.2.3.4 Maximum gate-gate voltage (for multiple-gate devices), under specified conditions.

5.2.3.5 For insulated-gate field-effect transistors with separate source and substrate terminals (chopper or analog-switch types):

- maximum gate-substrate voltage, under specified conditions;
- maximum drain-substrate voltage, under specified conditions;
- maximum source-substrate voltage, under specified conditions.

5.2.3.6 Drain current

5.2.3.6.1 Maximum drain current ($I_D$)

5.2.3.6.2 For power MOSFET only:

Maximum peak drain current ($I_{D_{\text{DM}}}$), under specified pulse conditions.

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</table>
5.2.3.7 Maximum forward gate current

5.2.3.8 Forward current of the inverse diode (for power MOSFET) in the following applications:
- low-frequency amplifier;
- switching transistor;
- chopper;
- low-level d.c. amplifier.

5.2.3.8.1 Maximum continuous (d.c.) source current ($I_{S(B)}$)

5.2.3.8.2 Maximum peak source current ($I_{SM(B)}$), under specified pulse conditions.

5.2.4 Mechanical data

The requirements for mechanical data, valid for other semiconductor devices, apply to these devices.

5.3 Characteristics

Characteristics are to be given at 25 °C, except where otherwise stated; other temperatures should be taken from the list in clause 5, chapter VI of IEC 60747-1.

5.3.1 Characteristics for low-frequency amplifier applications

5.3.1.1 Gate cut-off current

Gate leakage current

Maximum value, at specified gate-source or drain-gate voltage, other terminal connections being specified, at an operating temperature of 25 °C and at one specified higher operating temperature.

Together with:

Maximum value of the current of all gates connected together, at specified gate-source or drain-gate voltage, at an operating temperature of 25 °C and at one specified higher operating temperature.

5.3.1.2 Drain cut-off current

Maximum value, at specified drain-source and gate-source voltages, other terminal connections being specified, at an operating temperature of 25 °C and at one specified higher operating temperature.

5.3.1.3 Drain current at zero gate-source voltage ($I_{DSS}$)

Minimum and maximum values, for zero gate-source voltage, at a specified drain-source voltage, other terminal connections being specified, at an operating temperature of 25 °C and, where appropriate, at one specified higher operating temperature.
5.3.1.4 Drain current at specified gate-source voltage ($I_D$)
Minimum and maximum values. For specified gate-source and drain-source voltages, other terminal connections being specified, at an operating temperature of 25 °C and, where appropriate, at one specified higher operating temperature.

5.3.1.5 Gate-source cut-off voltage ($V_{GSoff}$)
Minimum and maximum values of gate-source voltage at which the drain current has been reduced to a specified low value, other terminal connections being specified, over the range of operating temperatures.

5.3.1.6 Gate-source threshold voltage ($V_{GS(TH)}$)
Minimum and maximum values, at a specified high value of drain-source voltage, and at a value of drain current equal to or more than 10 times the maximum value of drain current at zero gate voltage, other terminal connections being specified, at an operating temperature of 25 °C and, where appropriate, at one specified higher operating temperature.

5.3.1.7 Short-circuit input capacitance ($C_{iss}$)
Maximum small-signal value, in common-source configuration, under specified bias conditions and at a specified low frequency, with the output short-circuited to a.c.

5.3.1.8 Short-circuit output conductance and, where appropriate, capacitance ($g_{oss}$, $C_{oss}$)
Maximum small-signal value, in common-source configuration, under specified bias conditions and at a specified low frequency, with the input short-circuited to a.c.

5.3.1.9 Short-circuit feedback capacitance (where appropriate) ($C_{rss}$)
Maximum small-signal value, in common-source configuration, under specified bias conditions and at a specified low frequency, with the input short-circuited to a.c.

5.3.1.10 Forward transconductance ($g_{fs}$)

5.3.1.10.1 (Not applicable to power MOSFET)
Minimum and maximum values under specified bias conditions and at a specified low frequency.

5.3.1.10.2 For power MOSFET only
Minimum value, for specified drain-source voltage and drain current, at an operating temperature of 25 °C and, where appropriate, at a specified higher temperature.

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<th>TYPES</th>
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17
5.3.1.11 For low-noise applications, noise voltage and, where appropriate, noise figure ($V_n$, $F$):

Maximum value, in common-source configuration, under specified conditions of bias, source resistance, centre frequency and power bandwidth.

5.3.1.12 Characteristics of the inverse diode (for power MOSFET only)

5.3.1.12.1 Forward voltage ($V_{D(B)}$)

Maximum value at specified source current ($I_S(B)$) and at $V_{GS} = 0$.

5.3.1.12.2 Reverse recovery time ($t_{rr(B)}$)

Maximum value under specified conditions.

5.3.1.13 For power MOSFET only and when virtual channel temperature is quoted as a rating:

Thermal resistance channel-to-ambient or channel-to-case ($R_{th(j\text{-amb})}$) or ($R_{th(j\text{-case})}$).

Maximum value.

5.3.1.14 For power MOSFET only and when virtual channel temperature is quoted as a rating:

Transient thermal impedance channel-to-ambient or channel-to-case ($Z_{th(j\text{-amb})}$) or ($Z_{th(j\text{-case})}$).

Maximum value.

5.3.2 Characteristics for high-frequency amplifier applications

5.3.2.1 Gate cut-off current

Gate leakage current

Maximum value, at specified gate-source or drain-gate voltage, other terminal connections being specified, at an operating temperature of 25 °C and at one specified higher operating temperature.

Together with:

Maximum value of the current of all gates connected together, at specified gate-source or drain-gate voltage, at an operating temperature of 25 °C and at one specified higher operating temperature.

5.3.2.2 Drain cut-off current

Maximum value, at specified drain-source and gate-source voltages, other terminal connections being specified, at an operating temperature of 25 °C and at one specified higher operating temperature.

<table>
<thead>
<tr>
<th>TYPES</th>
<th>A</th>
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<tr>
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<td>+</td>
<td>+</td>
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</tbody>
</table>
5.3.2.3 Drain current at zero gate-source voltage ($I_{DS}$)

Minimum and maximum values, for zero gate-source voltage and a specified drain-source voltage, other terminal connections being specified, at an operating temperature of 25 °C and, where appropriate, at one specified higher operating temperature.

5.3.2.4 Drain current at specified gate-source voltage ($I_{D}$)

Minimum and maximum values, for specified drain-source voltage, other terminal connections being specified, at an operating temperature of 25 °C and, where appropriate, at one specified higher operating temperature.

5.3.2.5 Gate-source cut-off voltage ($V_{GS}$)

Minimum and maximum values of gate-source voltage at which the drain current has been reduced to a specified low value, other terminal connections being specified, over the range of operating temperatures.

5.3.2.6 Gate-source threshold voltage ($V_{GSO}$)

Minimum and maximum values, at a specified high value of drain-source voltage, and at a value of drain current equal to or more than 10 times the maximum value of drain current at zero gate voltage, other terminal connections being specified, at an operating temperature of 25 °C and, where appropriate, at one specified higher operating temperature.

5.3.2.7 $\gamma$-parameters

5.3.2.7.1 For all FETs under specified values of bias and frequency:

\begin{align*}
\gamma_{fs} & - \text{real and imaginary parts, maximum values;} \\
\gamma_{os} & - \text{real and imaginary parts, maximum values;} \\
\gamma_{fs} & - \text{real and imaginary parts, minimum and maximum values (see also 5.3.2.7.2);} \\
\gamma_{fs} & - \text{real and imaginary parts, maximum values;}
\end{align*}

5.3.2.7.2 For power MOSFET as alternative to $\gamma_{fs}$ transconductance ($g_{fs}$):

Minimum value, for specified drain-source voltage and drain current, at an operating temperature of 25 °C and, where appropriate, at a specified higher temperature.

5.3.2.8 Noise figure ($F$)

Maximum value, under specified conditions of bias, source impedance, centre frequency and power bandwidth. These conditions must be those which provide the lowest value of the noise figure.
5.3.2.9 For power MOSFET only and when virtual channel temperature is quoted as a rating:

Thermal resistance channel-to-ambient or channel-to-case (R\(_{th(j-amb)}\)) or (R\(_{th(j-case)}\)).

Maximum value.

5.3.2.10 For power MOSFET only and when virtual channel temperature is quoted as a rating:

Transient thermal impedance channel-to-ambient or channel-to-case (Z\(_{th(j-amb)}\)) or (Z\(_{th(j-case)}\)).

Maximum value.

5.3.3 Characteristics for switching applications

5.3.3.1 Gate cut-off current

Gate leakage current

Maximum value, at specified gate-source or drain-gate voltage, other terminal connections being specified, at an operating temperature of 25 °C and at one specified higher operating temperature.

Together with:

Maximum value of the current of all gates connected together, at specified gate-source or drain-gate voltage, at an operating temperature of 25 °C and at one specified higher operating temperature.

5.3.3.2 Drain cut-off current

Maximum value, at specified drain-source and gate-source voltages, other terminal connections being specified, at an operating temperature of 25 °C and at one specified higher operating temperature.

5.3.3.3 Gate-source cut-off voltage (V\(_{GSoff}\))

Minimum and maximum values of gate-source voltage at which the drain current has been reduced to a specified low value, other terminal connections being specified, over the range of operating temperatures.

5.3.3.4 Gate-source threshold voltage (V\(_{GSTD}\))

Minimum and maximum values, at a specified high value of drain-source voltage and at a value of drain current equal to or more than 10 times the maximum value of drain current at zero gate-voltage, other terminal connections being specified, at an operating temperature of 25 °C and, where appropriate, at one specified higher operating temperature.
5.3.3.5 On-state characteristics

5.3.3.5.1 Drain-source on-state voltage; \( (V_{DS(on)}) \)

Drain-source saturation voltage

Maximum value, at a specified large value of drain current and gate-source voltage, at an operating temperature of 25 °C and, where appropriate, at a specified higher temperature.

or (for power MOSFET only):

5.3.3.5.2 Drain-source on-state resistance \( (r_{DS(on)}) \)

Maximum value, at a specified large value of drain current and gate-source voltage, at an operating temperature of 25 °C and, where appropriate, at a specified higher temperature.

5.3.3.6 Small-signal gate-source capacitance at a specified frequency

a) Maximum value, under the electrical conditions specified in 5.3.3.1.

b) Where appropriate, maximum value, under the electrical conditions specified in 5.3.3.5 and with the drain-source voltage equal to the drain-source saturation voltage.

5.3.3.7 Small-signal drain-source capacitance at specified frequency

a) Maximum value under the electrical conditions specified in 5.3.3.1.

b) Where appropriate, maximum value under the electrical conditions specified in 5.3.3.5 and with the drain-source voltage equal to the drain-source saturation voltage.

5.3.3.8 Small-signal gate-drain capacitance at specified frequency

a) Maximum value under the electrical conditions specified in 5.3.3.1.

b) Where appropriate, maximum value under the electrical conditions specified in 5.3.3.5 and with the drain-source voltage equal to the drain-source saturation voltage.

5.3.3.9 Switching times (see figure 5)

They are stated under the following conditions:

a) common-source configuration;

b) specified condition in which output loading capacitance and resistance shall be included;

c) input pulse transition times, amplitude and repetition frequency to be specified;

d) \( V_{GS(off-state)} \) must be greater than or equal to the maximum gate-source cut-off voltage for type A and B devices, or lower than the minimum gate-source threshold voltage for type C devices;

e) \( V_{GS(on-state)} \) must correspond to a high drain current.

- Maximum values of: \( t_{(on)}, t_r, t_{(off)} \) and \( t_f \) separately.

NOTE Where \( t_{(off)} \) is only a small fraction of the total turn-off time \( (t_{off}) \), a maximum value for \( t_{off} \) alone is adequate.
5.3.3.10 Characteristics of the inverse diode (for power MOSFET) only

5.3.3.10.1 Forward voltage \( (V_D(B)) \)
Maximum value at specified source current \( (I_S(B)) \) and at \( V_{GS} = 0 \).

5.3.3.10.2 Reverse recovery time \( (t_{rr(B)}) \)
Maximum value under specified conditions.

5.3.3.10.3 Peak value of reverse recovery current \( (I_{SRRM}) \)
Maximum value under specified conditions.

5.3.3.11 For power MOSFET only and when virtual channel temperature is quoted as a rating:
Thermal resistance channel-to-ambient or channel-to-case \( (R_{th(j\text{-amb})}) \) or \( (R_{th(j\text{-case})}) \).
Maximum value.

5.3.3.12 For power MOSFET only and when virtual channel temperature is quoted as a rating:
Transient thermal impedance channel-to-ambient or channel-to-case \( (Z_{th(j\text{-amb})}) \) or \( (Z_{th(j\text{-case})}) \).
Maximum value.

5.3.4 Characteristics for chopper applications

5.3.4.1 Gate cut-off current
Gate leakage current
Maximum value, at specified gate-source or drain-gate voltage, other terminal connections being specified, at an operating temperature of 25 °C and at one specified higher operating temperature.

Together with:
Maximum value of the current of all gates connected together, at specified gate-source or drain-gate voltage, at an operating temperature of 25 °C and at one specified higher operating temperature.

5.3.4.2 Drain-source on-state voltage (saturation voltage) or drain-source on-state resistance.
Maximum value, at specified low values of drain current, for both polarities, and at a specified gate-source voltage.
5.3.4.3 Drain cut-off current or drain-source off-state resistance

Maximum value of drain-source cut-off current (or alternatively, minimum value of drain-source off-state resistance), at specified low values of drain-source voltage for both polarities and at a specified gate-source voltage.

<table>
<thead>
<tr>
<th>TYPES</th>
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</table>

![Figure 5 - Switching times](image-url)
5.3.4.4 Drain-source capacitance ($C_{ds}$)

Maximum value, at zero drain-source voltage and at a specified gate-source voltage or, where appropriate, source-case capacitance and drain-case capacitance.

5.3.4.5 Gate-drain capacitance ($C_{gd}$)

Maximum and, where appropriate, minimum value(s) at zero drain-source voltage and at a specified gate-source voltage.

5.3.4.6 Forward transconductance ($g_{fs}$) (for power MOSFET only)

Minimum value, for specified drain-source voltage and drain current, at an operating temperature of 25 °C and, where appropriate, at a specified higher temperature.

5.3.4.7 Characteristics of the inverse diode (for power MOSFET only)

5.3.4.7.1 Forward voltage ($V_{D(B)}$). Maximum value at specified source current ($I_{S(B)}$) and at $V_{GS} = 0$.

5.3.4.7.2 Reverse recovery time ($t_{rr(B)}$).

Maximum value under specified conditions.

5.3.4.8 For power MOSFET only and when virtual channel temperature is quoted as a rating:

Thermal resistance channel-to-ambient or channel-to-case ($R_{th(j-amb)}$) or ($R_{th(j-case)}$).

Maximum value.

5.3.4.9 For power MOSFET only and when virtual channel temperature is quoted as a rating:

Transient thermal impedance channel-to-ambient or channel-to-case ($Z_{th(j-amb)}$) or ($Z_{th(j-case)}$).

Maximum value.

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</table>
5.3.5 Characteristics for low-level d.c. amplifier applications

5.3.5.1 Gate cut-off current

Gate leakage current

Maximum value, at specified gate-source of drain-gate voltage, other terminal connections being specified, at an operating temperature of 25 °C and at one specified higher operating temperature.

Together with:

Maximum value of the current of all gates connected together, at specified gate-source or drain-gate voltage, at an operating temperature of 25 °C and at one specified higher operating temperature.

5.3.5.2 Drain cut-off current

Maximum value, at specified drain-source and gate-source voltages, other terminal connections being specified, at an operating temperature of 25 °C and at one specified higher operating temperature.

5.3.5.3 Drain current at zero gate-source voltage ($I_{DSS}$)

Minimum and maximum values, at a specified drain-source voltage, other terminal connections being specified, at an operating temperature of 25 °C and, where appropriate, at one specified higher operating temperature.

5.3.5.4 Drain current at specified gate-source voltage ($I_{DSX}$)

Minimum and maximum values, for specified gate-source and drain-source voltages, other terminal connections being specified, at an operating temperature of 25 °C and, where appropriate, at one specified higher operating temperature.

5.3.5.5 Gate-source cut-off voltage ($V_{GSOFF}$)

Minimum and maximum values of gate-source voltage at which the drain current has been reduced to a specified low value, other terminal connections being specified over the range of operating temperature.

5.3.5.6 Gate-source threshold voltage ($V_{GS(TO)}$)

Minimum and maximum values, at a specified high value of drain-source voltage and at a value of drain current equal to or more than 10 times the maximum value of drain current at zero gate voltage, other terminal connections being specified, at an operating temperature of 25 °C and, where appropriate, at one specified higher operating temperature.

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5.3.5.7 Noise voltage (where appropriate) \( (V_n) \)

Maximum value in common-source configuration, under specified circuit conditions.

5.3.5.8 Forward transconductance \( (g_{fs}) \) (for power MOSFET only)

Minimum value, for specified drain-source voltage and drain current, at an operating temperature of 25 °C and, where appropriate, at a specified higher temperature.

5.3.5.9 Characteristics of the inverse diode (for power MOSFET only)

5.3.5.9.1 Forward voltage \( (V_{D(B)}) \)

Maximum value at specified source current \( (I_{S(B)}) \) and at \( V_{GS} = 0 \).

5.3.5.9.2 Reverse recovery time \( (t_{rr(B)}) \)

Maximum value under specified conditions.

5.3.5.10 For power MOSFET only and when virtual channel temperature is quoted as a rating:

Thermal resistance channel-to-ambient or channel-to-case \( (R_{th(j-amb)}) \) or \( (R_{th(j-case)}) \).

Maximum value.

5.3.5.11 For power MOSFET only and when virtual channel temperature is quoted as a rating:

Transient thermal impedance channel-to-ambient or channel-to-case \( (Z_{th(j-amb)}) \) or \( (Z_{th(j-case)}) \).

Maximum value.

5.3.6 Characteristics for voltage-controlled resistor applications

5.3.6.1 Gate cut-off current

Gate leakage current

Maximum value, at specified gate-source or gate-drain voltage, other terminal connections being specified, at an operating temperature of 25 °C and at one specified higher operating temperature.

5.3.6.2 Small-signal drain-source resistance \( (r_{ds}) \)

Minimum and maximum small-signal values, at zero drain-source voltage and at two or more specified gate-source voltages, at an operating temperature of 25 °C and at one specified higher operating temperature.
5.3.6.3 Non-linearity distortion factor of drain-source small-signal resistance, where appropriate

Maximum value (total or individual harmonic contents), at specified drain-source and gate-source voltages and at specified drain-source a.c. signal, at an operating temperature of 25 °C and at one specified higher operating temperature.

5.3.6.4 Temperature coefficient of the small-signal drain-source resistance

Typical value.

5.3.6.5 Capacitances at a specified low frequency

a) Drain-source capacitance
   Maximum small-signal value, at zero drain-source voltage, at a specified gate-source voltage, with the gate short-circuited for a.c. to the source.

b) Drain-gate capacitance
   Maximum small-signal value at zero drain-source voltage, at a specified gate-source voltage, with the gate short-circuited for a.c. to the source.

c) Gate-source capacitance (where appropriate)
   Maximum small-signal value at zero drain-source voltage, at a specified gate-source voltage, with the drain short-circuited for a.c. to the source.

5.3.6.6 Forward transconductance ($g_{fs}$) (for power MOSFET only)

Minimum value, for specified drain-source voltage and drain current, at an operating temperature of 25 °C and, where appropriate, at a specified higher temperature.

5.3.6.7 For power MOSFET only and when virtual channel temperature is quoted as a rating:

Thermal resistance channel-to-ambient or channel-to-case ($R_{th(j-amb)}$) or ($R_{th(j-case)}$).

Maximum value.

5.3.6.8 For power MOSFET only and when virtual channel temperature is quoted as a rating:

Transient thermal impedance channel-to-ambient or channel-to-case ($Z_{th(j-amb)}$) or ($Z_{th(j-case)}$).

Maximum value.
5.3.7 Specific characteristics of matched-pair field-effect transistors for low-frequency differential applications

5.3.7.1 Difference of gate cut-off currents

Difference of gate leakage currents \((I_{G1} - I_{G2})\)

Maximum absolute value, at specified drain-gate or drain-source voltage and drain current.

5.3.7.2 Ratio of drain currents

5.3.7.2.1 Ratio of drain currents for zero gate-source voltage \(\left(\frac{I_{DS1}}{I_{DS2}}\right)\)

Minimum value of the ratio of the drain currents, at a specified drain-source voltage and zero gate-source voltage.

5.3.7.2.2 Ratio of drain currents for specified gate-source voltage

Minimum value of the ratio of the drain currents, at specified drain-source and gate-source voltages.

NOTE This ratio should be stated as the smaller value divided by the larger value.

5.3.7.3 Difference of small-signal common-source output conductances, where appropriate \(\left(\frac{g_{os1}}{g_{os2}}\right)\)

Maximum absolute value of the difference of the output conductances, at specified drain-gate or drain-source voltage, drain current, and frequency.

5.3.7.4 Ratio of small-signal common-source forward transconductances \(\left(\frac{g_{fs1}}{g_{fs2}}\right)\)

Minimum value of the ratio of forward transconductances, at specified drain-gate or drain-source voltage, drain current, and frequency

NOTE This ratio should be stated as the smaller value divided by the larger value.

5.3.7.5 Difference of gate-source voltages \(\left(V_{GS1} - V_{GS2}\right)\)

Maximum absolute value of the difference of the gate-source voltages, at specified drain-gate or drain-source voltage and drain current.

5.3.7.6 Change in difference of gate-source voltages between two temperatures \(\left(\frac{\Delta(V_{GS1} - V_{GS2})}{\Delta T}\right)\)

Maximum absolute value of the change of the difference of the gate-source voltages (as in 5.3.7.5) between two specified temperatures, at the same specified drain-gate or drain-source voltage and drain current.
5.4 Application data

5.4.1 Intermodulation and AGC

For high-frequency applications and for all three categories of devices, some indication of the intermodulation and AGC characteristics, appropriate to the intended device application, must be given. This should cover a suitable range of source currents and frequencies.

6 Measuring methods

6.1 General

6.1.1 Polarity

The polarities of the power supplies, shown in the circuits in this standard, are applicable to N-channel type devices. However, the circuits can be adapted for P-channel type devices by changing the polarities of the meters and the power supplies.

6.1.2 General precautions

The general precautions listed in clause 1, chapter VII of IEC 60747-1 apply. In addition, special care should be taken to use low-ripple d.c. supplies and to decouple adequately all bias supply voltages at the frequency of measurement.

For four-terminal devices, the fourth terminal should be connected as specified.

6.1.3 Handling precautions

Because of the very high input resistance of field-effect transistors, the gate insulation layer (for insulated-gate types) or the gate junction (for junction-gate types) may be irreversibly damaged if an excessive voltage is allowed to build up, e.g. due to contact with electrostatically charged persons, leakage currents from soldering irons, etc.

When handling these devices, the handling precautions given in clause 1, chapter IX, of IEC 60747-1.

6.1.4 Type categories

See clause 3.

6.2 Gate cut-off current or gate leakage current

6.2.1 Gate cut-off current of junction-gate type (type A)

6.2.1.1 Purpose

To measure the gate cut-off current of a junction-gate field-effect transistor, under specified conditions.
6.2.1.2 Circuit diagram

![Diagram](image)

Figure 6 – Basic circuit for the measurement of gate cut-off current

6.2.1.3 Measurement procedure

The drain-source voltage is set to the specified value (if this voltage is specified as zero, drain and source terminals should be short-circuited). The gate cut-off current is measured at the specified gate-source voltage, using a sensitive ammeter for $I_G$.

6.2.1.4 Specified conditions
- Ambient or reference-point temperature.
- Gate-source voltage.
- Drain-source voltage.

6.2.2 Gate leakage current of insulated-gate type (types B and C)

6.2.2.1 Purpose

To measure the leakage current of an insulated-gate field-effect transistor, under specified conditions.

6.2.2.2 Circuit diagram

![Diagram](image)

Figure 7 – Basic circuit for the measurement of gate leakage current
6.2.2.3 Circuit description and requirements

The source and substrate terminals are connected together. $R$ is a protective resistor. The value of resistor $R_1$ should be smaller than $V_{GS}/100$ $I_{GS_{\max}}$. Voltmeter $V_1$ should have a high sensitivity and an input resistance of more than 100 times $R_1$. The gate leakage current is given by:

$$I_{GS} = \frac{V_1}{R_1}$$

6.2.2.4 Precautions to be observed

a) The entire circuit should be placed inside an electrostatic screen.
b) Special care should be taken to avoid incorrect measurements caused by leakage currents occurring between the gate terminal and any other node in the circuit.

6.2.2.5 Measurement procedure

The drain-source voltage is adjusted to the specified value.

The voltage $V_1$ is measured at the specified gate-source voltage and the value of gate leakage current is calculated.

6.2.2.6 Specified conditions

- Ambient or reference-point temperature.
- Gate-source voltage.
- Drain-source voltage.

6.3 Drain current (types A, B and C) ($I_D$)

6.3.1 Purpose

To measure the drain current of a field-effect transistor, under specified conditions.

6.3.2 Circuit diagram

![Figure 8 - Basic circuit for the measurement of drain current](image)

6.3.3 Circuit description and requirements

$R$ is a protective resistor.

6.3.4 Precautions to be observed

See general precautions.
6.3.5 Measurement procedure
The specified gate-source voltage is applied to the gate. If this voltage is specified as zero, the gate should be short-circuited to the source.

The drain current is measured at the specified drain-source voltage.

6.3.6 Specified conditions
- Ambient or reference-point temperature.
- Gate-source voltage.
- Drain-source voltage.

6.4 Drain cut-off current (types A, B and C)

6.4.1 Purpose
To measure the drain cut-off current of a field-effect transistor, under specified conditions.

6.4.2 Circuit diagram
The circuit of figure 8 may be used for this measurement.

6.4.3 Precautions to be observed (for types B and C)
The entire circuit should be placed inside an electrostatic screen.

6.4.4 Measurement procedure
The drain current is chosen so that the device is operating in the cut-off region.

6.4.5 Specified conditions
- Ambient or reference-point temperature.
- Gate-source voltage.
- Drain-source voltage.

6.5 Gate-source cut-off voltage (types A and B) ($V_{GS_{on}}$)

6.5.1 Purpose
To measure the gate-source cut-off voltage, under specified conditions.

6.5.2 Circuit diagram
The circuit of figure 8 may be used for this measurement.

6.5.3 Precautions to be observed
The entire circuit should be placed inside an electrostatic screen.
6.5.4 Measurement procedure
The specified drain-source voltage is applied.

NOTE An additional substrate-source voltage may be applied if necessary.

The gate-source voltage is adjusted to obtain the specified drain current in the cut-off region. This is the required value of the gate-source cut-off voltage.

6.5.5 Specified conditions
- Ambient or reference-point temperature.
- Drain-source voltage.
- Drain current.

6.6 Gate-source threshold voltage (type C) \( (V_{GS(TH)}) \)

6.6.1 Purpose
To measure the gate-source threshold voltage, under specified conditions.

6.6.2 Circuit diagram
The circuit of figure 8 with suitable shield may be used for this measurement, except that the polarity of the gate-source voltage should be reversed.

6.6.3 Precautions to be observed
The entire circuit should be placed inside an electrostatic screen.

6.6.4 Measurement procedure
The specified drain-source voltage is applied.

The gate-source voltage is adjusted to obtain the specified drain current. This is the required value of the gate-source threshold voltage.

6.6.5 Specified conditions
- Ambient or reference-point temperature.
- Drain-source voltage.
- Drain current.

6.7 Small-signal short-circuit input capacitance (types A, B and C) \( (C_{iss}) \)

6.7.1 Purpose
To measure the small-signal input capacitance of a field-effect transistor, under specified conditions.
6.7.2 Circuit diagram

![Circuit Diagram](image)

Figure 9 – Basic circuit for the measurement of small-signal short-circuit input capacitance

6.7.3 Circuit description and requirements

A capacitance bridge is used for this measurement.

If the bridge cannot (or should not) pass d.c., the alternative (shunt) bias circuit shown in figure 10 may be used.

![Circuit Diagram](image)

Figure 10 – Alternative circuit for measurement of small-signal short-circuit input capacitance

Capacitances $C_1$ and $C_2$ should present short circuits at the measurement frequency, satisfying the following conditions:

$$\omega C_1 \gg |Y_{IS}|$$
$$\omega C_2 \gg |Y_{OS}|$$
6.7.4 Precautions to be observed
See general precautions.

6.7.5 Measurement procedure
With no device in the measurement socket, the zero adjustments of the bridge are made.

The device to be measured is then inserted into the measurement socket. The drain-source voltage ($V_{DS}$) and the gate-source voltage ($V_{GS}$) are adjusted to obtain the specified bias conditions.

The bridge is rebalanced, and the change in the capacitance reading is the value of the small-signal short-circuit input capacitance.

6.7.6 Specified conditions
- Drain-source voltage.
- Gate-source voltage.
- Frequency of measurement.

6.8 Small-signal short-circuit output conductance (type A, B and C) ($g_{oss}$)

6.8.1 Purpose
To measure the small-signal output conductance, under specified conditions.

6.8.2 General
Two alternative circuits are described, one using a null method, the other using the two-voltmeter principle.

The first method requires an admittance bridge but has the advantage that $g_{oss}$ may be measured at high and low frequencies, and that both $g_{oss}$ and $C_{oss}$ may be measured simultaneously.

The second method simply measures the modulus of $Y_{os} = g_{oss} + jωC_{oss}$ which is identical with $g_{oss}$ for sufficiently low frequency.

6.8.3 Null method

6.8.3.1 Circuit diagram

![Figure 11 – Basic circuit for the measurement of the output conductance $g_{oss}$ (null method)](null)
6.8.3.2 Circuit description and requirements

The admittance bridge is used for this measurement.

Capacitances $C_1$ and $C_2$ should present short circuits at the measurement frequency, satisfying the following conditions:

$$\omega C_1 >> |y_{is}|$$
$$\omega C_2 >> |y_{os}|$$

6.8.3.3 Precautions to be observed

See general precautions.

6.8.3.4 Measurement procedure

With no device in the measurement socket, the zero adjustments of the bridge are made.

The device to be measured is then inserted into the measurement socket; the drain-source voltage ($V_{DS}$) and the gate-source voltage ($V_{GS}$) are adjusted to obtain the specified bias conditions with the push-button P closed.

With the push-button P open, the bridge is rebalanced, and the values of $g_{oss}$ or $\text{Re} (y_{os})$ and $\text{Im} (y_{os})$, if needed, are then read.

6.8.3.5 Specified conditions

- Drain-source voltage.
- Gate-source voltage or drain current.
- Frequency of measurement.

6.8.4 Two-voltmeter method

6.8.4.1 Circuit diagram

![Basic circuit for the measurement of the output conductance $g_{oss}$ (two-voltmeter method)](image)

$P = \text{push-button}$

*Figure 12 – Basic circuit for the measurement of the output conductance $g_{oss}$ (two-voltmeter method)*
6.8.4.2 Circuit description and requirements

All bias voltages applied should be adequately decoupled at the frequency of measurement.

The value of $\omega C_1$ should be much larger than $|\gamma_{ds}|$; the value $\omega C_2$ should be high.

Inductance $L$ is optional; its use facilitates the adjustment of the specified operating point.

Resistor $R_1$ should be sufficiently low with respect to $\frac{1}{g_{oss}}$; practically, a value of 10 $\Omega$ to 100 $\Omega$, will be used, in accordance with the voltmeter sensitivity.

The a.c. voltmeter should have sufficient sensitivity; for the measurement or low conductances, it should preferably be a selective instrument.

6.8.4.3 Precautions to be observed

See general precautions.

6.8.4.4 Measurement procedure

The device to be measured is inserted into the measurement socket; the drain-source voltage ($V_{DS}$) and the gate-source voltage ($V_{GS}$) are adjusted to obtain the specified bias conditions with the push-button $P$ closed.

With the switch $S$ in position 1, the value $V_1 = I_d R_1$ is measured, while with the switch $S$ in position 2, the value $V_2 = V_{ds} + I_d R_1$ is measured.

Thus:

$$V_2 - V_1 = V_{ds}$$

$$I_d = \frac{V_1}{R_1}$$

$$|y_{os}| = \frac{V_1}{R_1 (V_2 - V_1)} \approx \frac{V_1}{R_1 V_2} \quad (\text{for } V_2 \gg V_1)$$

For sufficiently low frequencies: $|y_{os}| \leq g_{oss}$.

6.8.4.5 Specified conditions

- Drain-source voltage.
- Gate-source voltage or drain current.
- Frequency of measurement.

6.9 Small-signal short-circuit output capacitance (type A, B and C) ($C_{oss}$)

6.9.1 Purpose

To measure the small-signal short-circuit output capacitance, under specified conditions.
6.9.2 General

As mentioned in 6.8.2 and 6.8.3.2, the method of 6.8.3 may also be used for the measurement of $C_{oss}$. However, it is often preferable to use a separate method of measurement for $C_{oss}$, especially when the method of 6.8.4 is used for the measurement of $g_{oss}$.

6.9.3 Circuit diagrams

![Figure 13 - Basic circuit for measurement of short-circuit output capacitance](image)

If the capacitance bridge cannot (or should not) carry d.c., the alternative circuit shown in figure 14, should be used.

![Figure 14 - Alternative circuit for measurement of short-circuit output capacitance](image)

6.9.4 Circuit description and requirements

A capacitance bridge is used, thus making it possible to apply a null method. $C_2$ should be much larger than $C_{oss}$ and $\omega C_1$, much larger than $|y_{le}|$.

The impedance of $L$ should be sufficiently high, so that it is possible to compensate it by the bridge adjustments. The d.c. resistance should be low compared to the output resistance of the device. Alternatively, a suitable tuned parallel resonant circuit (or, at very low drain currents, a suitable resistor) may be used.

6.9.5 Precautions to be observed

See general precautions.
6.9.6 Measurement procedure

With no device in the measurement socket, the zero adjustments of the capacitance bridge are made.

The device to be measured is then inserted into the measurement socket; $V_{DS}$ and $V_{GS}$ (or $I_D$) are adjusted to the specified values.

The bridge is rebalanced; the difference of the capacitance readings of this adjustment and that with no device in the measurement socket yields the value of $C_{oss}$.

6.9.7 Specified conditions

- Drain-source voltage.
- Gate-source voltage or drain current.
- Frequency of measurement.

6.10 Small-signal short-circuit forward transconductance (types A, B and C)

6.10.1 Purpose

To measure the small-signal short-circuit forward transconductance, under specified conditions.

6.10.2 General

Two alternative circuits are described, one using a null method, the other using the two-voltmeter principle.

- The first method needs a three-pole transfer admittance bridge, but has the advantage that $g_{fs}$ may be measured at low frequencies, as well as $Y_{fs} = g_{fs} + j\omega C_{gs}$ at high frequencies. Furthermore, it guarantees a real short circuit at the output.
- The second method simply measures the modulus of $Y_{fs}$, which is identical with $g_{fs}$ for sufficiently low frequencies.

6.10.3 Null method

6.10.3.1 Circuit diagram

![Circuit diagram for small-signal short-circuit forward transconductance](image)

Figure 15 – Circuit for the measurement of short-circuit forward transconductance $g_{fs}$
6.10.3.2 Circuit description and requirements

All bias supply voltages applied should be adequately decoupled at the frequency of measurement.

The value of $\omega C_1$ should be much larger than $|y_{IS}|$ and the value of $\omega C_2$ should be much larger than $|y_{OS}|$.

$R_1$ should be much larger than the internal impedance of the bridge, in order not to affect the measurement accuracy.

$R_2$ should be much larger than the internal resistance of the detector, but nevertheless sufficiently lower than $1/y_{IS}$, in order not to affect the measurement sensitivity.

The values of $\omega C_3$ and $\omega C_4$ should be much larger than $|y_{IS}|$ to be measured.

The internal resistance of the voltmeter $V_{os}$ should be much larger than $V_{DS}/I_D$.

6.10.3.3 Precautions to be observed

See general precautions.

6.10.3.4

With no device in the measurement socket, the zero adjustments of the bridge are made.

The device to be measured is then inserted into the measurement socket; $V_{DS}$ and $V_{GS}$ (or $I_D$) are adjusted to the specified values.

The bridge is rebalanced, and the values of $g_{fs}$, or Re ($y_{fs}$) and Im ($y_{fs}$) if needed, are then read.

6.10.3.5 Specified conditions

- Drain-source voltage.
- Gate-source voltage or drain current.
- Frequency of measurement.
6.10.4 Two-voltmeter method

6.10.4.1 Circuit diagram

Figure 16 – Circuit for the measurement of forward transconductance $g_{fs}$
(two-voltmeter method)

6.10.4.2 Circuit description and requirements

A suitable oscillator should be used, the frequency of which should be sufficiently low.

The value of resistor $\omega C_3$ and $\omega C_2$ should be much greater than $1/R_0$. The value of $\omega C_1$ should be high.

The value of resistor $R_G$ is not critical; it should preferably not be too high.

Resistance $R_G$ must be low compared with $\frac{1}{|\gamma_{os}|}$.

Voltmeter V (see figure 16) should have sufficient sensitivity; for the measurement of low values of $g_{fs}$, it should preferably be a selective instrument.

6.10.4.3 Precautions to be observed

See general precautions.

6.10.4.4 Measurement procedure

The device to be measured is inserted into the measurement socket; $V_{DS}$ and $V_{GS}$ (or $I_D$) are adjusted to the specified values.

With the switch S in position 1, the value $V_1 = V_{gs}$ is measured, while with the switch S in position 2, the value $V_2 = V_{ds} + I_d R_d$ is measured.

Thus:

$$|\gamma_{fs}| = \frac{I_d}{V_{gs}} = \frac{V_2}{V_1 R_d}$$

For sufficiently low frequencies: $|\gamma_{fs}| \approx g_{fs}$. 

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6.10.4.5 Specified conditions
- Drain-source voltage.
- Gate-source voltage or drain current.
- Frequency of measurement.

6.11 Small-signal short-circuit feedback capacitance (types A, B and C) \((C_{rs})\)

6.11.1 Purpose
To measure the small-signal short-circuit feedback capacitance, under specified conditions.

6.11.2 Circuit diagram

6.11.2.1 Figure 17 shows an example of the circuit to be used. A differential transformer bridge is used.

![Circuit diagram of feedback capacitance measurement](image)

Figure 17 – Circuit for measurement of feedback capacitance \(C_{rs}\)

6.11.2.2 If the bridge cannot (or should not) pass d.c., the alternative circuit shown in figure 18, should be used.
Figure 18 – Circuit for measurement of feedback capacitance \( C_{rs} \)
(when the bridge cannot pass d.c.)

Equivalent circuit

Evaluation of the equivalent circuit for \( V_n = 0 \) yields:

\[
y_{rs} = y_B
\]

6.11.3 Circuit description and requirements

Capacitances \( \omega C_1 \) should be much larger than \( |y_{rs}| \) and \( \omega C_2 \) much larger than \( |y_{os}| \).

Resistor \( R_2 \): the value of this resistor should not be too high. It may be preferable to shunt it by an adequate inductance \( L \).

6.11.4 Precautions to be observed

See general precautions.
6.11.5 Measurement procedure

With no device in the measurement socket, the bridge is initially balanced.

The device is inserted into the measurement socket and the operating point adjusted to the specified values $V_{DS}$ and $V_{GS}$ (or $I_D$).

The bridge is again adjusted for balance. The reading of $y_B$ for this adjustment minus the reading of the initial adjustment yields:

$$y_{rs} = g_{rs} + j\omega C_{rs}$$

6.11.6 Specified conditions

- Drain-source voltage.
- Gate-source voltage or drain current.
- Frequency of measurement.

6.12 Noise (types A, B and C) ($F, V_n$)

6.12.1 Purpose

To measure the equivalent input noise voltage or noise factor, under specified conditions.

6.12.2 Equivalent input noise voltage

6.12.2.1 Circuit diagram

A circuit in accordance with the block diagram shown in figure 20 should be used.

![Block diagram for the measurement of equivalent input noise voltage](image)

Figure 20 – Block diagram for the measurement of equivalent input noise voltage

Figure 21 shows an example of a circuit in accordance with that block diagram.
6.12.2.2 Circuit description and requirements

The frequency of the generator should be adjusted to be the centre frequency of the selective amplifier. The output voltage should be adjusted in such a way that the input voltage to the transistor is high compared with the noise voltage, but low enough to avoid overloading of the device.

The voltage dividing ratio of the voltage divider \(R_2, R_1\) should be known.

For the bias source, special care should be taken to achieve low-noise biasing (especially important for the gate bias).

All resistors that might deliver noise to the circuit should be of a low-noise type (e.g. metallic film resistors).

A neutralization network should be used, when appropriate.

Adequate shielding to minimize the influence of external electromagnetic fields should be provided, when appropriate.

The amplifier should be linear up to a level of at least 20 dB higher than the r.m.s. noise value, so that noise peaks are correctly amplified.

The second stage noise should be as low as possible. The noise level measured with the device removed from the circuit should be at least 15 dB lower than that measured with the device in the circuit.

The output voltmeter should measure the true r.m.s. value.

The equivalent noise bandwidth should be accurately known.

\(\omega C_3\) should be much larger than \(1/R_3\) and \(\omega C_2\) much larger than \(1/R_2\).
6.12.2.3 Precautions to be observed

See general precautions.

6.12.2.4 Measurement procedure

The device is inserted into the measurement socket and the operating point is adjusted to the specified values of $V_{OS}$ and $V_{GS}$ (or $I_D$).

The input voltage $V_i$ is adjusted to a suitable value (e.g. 0.1 V).

With switch $S$ in position 1, the output voltage $V_{o1}$ is measured, after proper adjustment of the gain of the amplifier.

With switch $S$ in position 2, the output voltage $V_{o2}$ is measured.

The noise voltage is given by:

$$V_n = \frac{V_{o2}}{V_{o1}} \frac{R_2}{R_1 + R_2}$$

6.12.2.5 Specified conditions

- Ambient or reference-point temperature.
- Values of resistors $R_1$ and $R_2$.
- Drain-source voltage.
- Gate-source voltage or drain current.
- Frequency of measurement and bandwidth.

6.12.3 Noise factor

All methods of measurement for bipolar transistors (see 6.1.14 of IEC 60747-7), are applicable for field-effects transistors.

6.12.4 Relation between equivalent input noise voltage and noise factor

If a resistor $R_g$ is inserted between the input terminals, the overall noise voltage is given by:

$$V_{n_{tot}} = \sqrt{V_n^2 + 4kT R_g \Delta f}$$

From this, the general formula for the noise factor yields:

$$F = \sqrt{\frac{V_n^2 + 4kT R_g \Delta f}{4kT R_g \Delta f}}$$

The formula for $V_{n_{tot}}$ yields a possibility for measuring $V_n$ directly.

The generator is disconnected from the circuit and $R_2$ is replaced.

With $R_g$ short-circuited, the resulting output voltage is measured.

removed and $R_g$ is adjusted to yield an output voltage twice higher.

Then:

$$V_n = \sqrt{4kT R_g \Delta f}$$
6.13 \( y \)-parameters (types A, B and C)

Some of the low frequency and intermediate frequency \( y \)-parameters can be measured, as indicated in this standard. For the \( y \)-parameters for high frequency, all methods of measurement for bipolar transistors (see 6.1.13 of IEC 60747-7) are applicable for field-effect transistors.

6.14 Switching times (types A, B and C) \((t_{on}, t_{off})\)

6.14.1 Purpose

To measure the various switching times, under specified conditions.

6.14.2 General

As a rule, the turn-on time \((t_{on})\) and the turn-off time \((t_{off})\) should be measured as the switching times. Unless otherwise specified, the common-source configuration is used.

6.14.3 Circuit diagram

![Circuit diagram for measurement of switching times](image)

Figure 22 – Circuit for measurement of switching times

6.14.4 Circuit description and requirements

The internal resistance of the bias supply \( V_{GG} \) should be smaller than 0.01 \( R_g \), where \( R_g \) is the equivalent internal resistance of the pulse generator. The internal resistance of the bias supply \( V_{DD} \) should be smaller than 0.01 \( R_L \).

The pulse width of the pulse generator should be much greater than the turn-on and the turn-off times of the device to be measured; the duty cycle should be low (about 1 \%).

The rise and fall times of the pulse should be less than 0.25 of the rise and fall times of the device to be measured.

A double-beam oscilloscope should be used; its rise time should be less than 0.25 of the rise time of the device to be measured.
6.14.5 Precautions to be observed

See general precautions.

6.14.6 Measurement procedure

The device to be measured is inserted into the measurement socket. The voltages $V_{GG}$ and $V_{DD}$ are adjusted to the specified values.

The specified input voltage $V_p$ is applied by means of the pulse generator.

The input and output waveforms are displayed on the oscilloscope and the turn-on and the turn-off times are measured in accordance with figure 23.

![Figure 23 - Waveforms in the measurement of switching times](image)

6.14.7 Specified conditions

- Ambient or reference-point temperature.
- Supply voltages.
- Values of $R_L$ and $C_L$.
- Input pulse conditions:
  - amplitude $V_p$;
  - duration;
  - repetition frequency;
  - rise and fall times.
6.15 Static drain-source on-state resistance ($r_{DSon}$) or drain-source on-state voltage ($V_{DSon}$) and off-state resistance ($r_{DSoff}$)

6.15.1 Purpose

To measure drain-source on-state resistance or drain-source on-state voltage, and off-state resistance, under specified conditions.

6.15.2 General

As a rule, $r_{DSon}$ and $r_{DSoff}$ are expressed in terms of d.c. resistance, under conditions of saturation and cut-off respectively, as shown in figure 24. Unless otherwise specified, the common-source configuration is used.

![Figure 24](image)

6.15.3 Circuit diagram

![Figure 25](image)

6.15.4 Circuit description and requirements

The internal resistance of the voltmeter should be much higher than the on-state and off-state resistances to be measured.

6.15.5 Precautions to be observed

See general precautions.
6.15.6 Measurement procedure

6.15.6.1 On-state and off-state resistances

The device to be measured is inserted into the measurement socket; \( V_{DS} \) and \( V_{GS} \) are adjusted to the specified values.

The drain current \( I_D \) is measured, and the on-state and off-state resistances are calculated by means of the following equations:

\[
\begin{align*}
    r_{D\text{on}} &= \frac{V_{DS1}}{I_D1} \\
    r_{D\text{off}} &= \frac{V_{DS2}}{I_D2}
\end{align*}
\]

6.15.6.2 Drain-source on-state voltage

The device to be measured is inserted into the measurement socket; \( V_{GS} \) and \( I_D \) are adjusted to the specified values.

The measured value of \( V_{DS} \) is then the required value of the on-state voltage.

6.15.7 Specified conditions

- Ambient or reference-point temperature.
- Drain-source voltage or drain current.
- Gate-source voltage.

6.16 On-state drain-source resistance (under small-signal conditions) \( (r_{ds(on)}) \)

6.16.1 Purpose

To measure the on-state drain-source resistance, by means of a low-frequency bridge.

6.16.2 Circuit diagram

![Circuit diagram](image)

Figure 26

6.16.3 Circuit description and requirements

The bridge should be able to pass d.c.

For type B and C devices, the case and/or substrate should be connected to the source.
6.16.4 Precautions to be observed

See general precautions.

6.16.5 Measurement procedure

The bridge is first balanced without the transistor.

The transistor is then inserted into the measurement socket and the gate-source voltage is adjusted to the specified value. The bridge is rebalanced, and the value of the on-state resistance is read from the bridge.

6.16.6 Specified conditions

- Drain-source voltage (equal to zero).
- Gate-source voltage.
- Frequency (1 kHz, unless otherwise specified).

NOTE The bridge may be replaced by an a.c. voltmeter, a.c. ammeter and signal generator, if desired.

6.17 Scattering parameters

See subclause 6.1.13.6 of IEC 60747-7.

6.18 Channel-case transient thermal impedance ($Z_{thJC}$) and thermal resistance ($R_{thJC}$) of a power field-effect transistor

6.18.1 Purpose

To measure the channel-case transient thermal impedance and channel-case thermal resistance of a power field-effect transistor.

This method cannot be used if an isolation material is used having a varying temperature coefficient, e.g. beryllium oxide.

6.18.2 Cooling method

6.18.2.1 Principle of the method

As a temperature-sensitive characteristics, the forward voltage of the inverse diode ($V_{SD}$ in figure 27) is chosen to be measured at a fixed reference current ($I_M$ in figure 27). After a heating current has been applied and thermal equilibrium is established, the heating current is switched off. During the following cooling period, $V_{SD}$ and the case temperature are recorded as a function of time. From the recorded values and the initial heating power, the values of $Z_{thJC}$ and $R_{thJC}$ are determined by means of a calibration curve.
6.18.2.2 Circuit diagram

![Circuit Diagram]

Figure 27 – Circuit diagram

6.18.2.3 Circuit description and requirements

- $V_{GG}$ = adjustable voltage source
- $V_{DD}$ = adjustable voltage source
- $I_M$ = reference (direct) current generator
- $S_1, S_2$ = synchronous switches
- $M_A, M_B$ = recording equipment (e.g. dual-beam oscilloscope) to record $V_{DS}$ and $I_D$ or $V_{SD}$ and $I_M$
- $R_L$ = limiting resistors for drain current $I_D$
- $R_G$ = protective resistor
- $R_S$ = measuring resistor for $I_D$ and $I_M$

6.18.2.4 Precautions to be observed

Care must be taken that the drain-source channel is not conducting when the forward voltage of the inverse diode is measured. In the example, this is reached by setting $V_{GS}$ equal to zero. Make sure that switch $S_2$ is in position 1 before $S_1$ is switched to position 1.

The change-over time of switches $S_1, S_2$ shall be short enough so that $Z_{th JC}$ can, (at least by interpolation back to $t = 0$), be measured for the shortest required cooling period $t_c$.

$I_M$ should be sufficiently small so that the corresponding power $P(M) = I_M \cdot V_{SD}$ is relatively small compared to the heating power $P(H) = I_D \cdot V_{DS}$ or may even be neglected (see equation (1) in 6.18.2.5).
6.18.2.5 Measurement procedure

A thermosensor is fixed at the reference point of the transistor being measured to measure its case temperature $T_c$. A calibration curve is established as follows: the transistor is externally heated to rising step values of case temperature $T_c^*$. At each step, after thermal equilibrium has been reached, the forward voltage of the inverse diode $V_{SD}$ is measured. From the measured values, the calibration curve $T_c^* = f(V_{SD})$ is established.

With the switches in position 2, the heating power $P(H) = I_D \cdot V_{DS}$ is set to the intended value, and this setting is subsequently maintained. $P(H)$ is recorded. After thermal equilibrium has been reached, the case temperature $T_c(0)$ and the forward voltage of the inverse diode $V_{SD}(0)$ are recorded.

Switching back to position 1, the heating process is interrupted, and the courses $V_{SD}(t)$ and $T_c(t)$ during the cooling process are recorded.

By means of the calibration curve, the recorded values of $V_{SD}(0)$ and $V_{SD}(t)$ are converted to the corresponding values of $T_c^*(0)$ and $T_c^*(t)$ respectively.

The channel-case transient thermal impedance after a particular cooling period $t_c$ is calculated as:

$$Z_{thc}(t_c) = \frac{[T_c^*(0) - T_c^*(t_c)] [T_c^*(0) - T_c(0)]}{P(H) - P(M)}$$

where

$T_c^*(0), T_c^*(t_c)$ are the values taken from the calibration curve for $V_{SD}(0)$ and $V_{SD}(t_c)$;

$T_c(0), T_c(t_c)$ are the values of $T_c$ at $t = 0$ and $t = t_c$ respectively;

$P(H) = I_D \cdot V_{DS}$ is the heating power in position 2;

$P(M) = I_M \cdot V_{SD}$ is the measuring power in position 1.

The channel-case thermal resistance $R_{thc}$ is the value finally reached of $Z_{thc}$ after the cooling period is settled, i.e. thermal equilibrium has again been reached.

6.18.3 Heating method

6.18.3.1 Principle of the method

As a temperature-sensitive characteristic, the forward voltage of the inverse diode ($V_{SD}$ in figure 28) is chosen to be measured at a fixed reference current ($I_M$ in figure 28). Starting from thermal equilibrium at heating current zero, a heating current is applied to specified values of heating power and duration. The values of $V_{SD}$ and of the case temperature are measured just before and after the application of heating current. From the measured values of $V_{SD}$, the channel temperature may be determined from the calibration curve. The values of $Z_{thc}$ and $R_{thc}$ may then be calculated using the values of heating power, channel temperature and reference-point temperature.
6.18.3.2 Circuit diagram

Same as in 6.18.2.2.

6.18.3.3 Circuit description and requirements

Same as in 6.18.2.3.

6.18.3.4 Precautions to be observed

Same as in 6.18.2.4 but with reference to equation (2) in 6.18.3.5.

6.18.3.5 Measurement procedure

A thermosensor is fixed at the reference point of the transistor being measured to measure its case temperature $T_c$.

A calibration curve is established as described in 6.18.2.5.

With the switches in position 2, the heating power $P(H) = I_D \cdot V_{DS}$ is set to the intended value and this setting is subsequently maintained. $P(H)$ is recorded.

The heating power is switched off by switching back to position 1.

When thermal equilibrium has been reached, the case temperature $T_c(0)$ and the forward voltage of the inverse diode $V_{SD}(0)$ are recorded.

By switching first to position 2 and then back to position 1, the heating power is applied for the intended heating period $t_h$.

Immediately after having switched back to position 1, the case temperature $T_c(t_h)$ and the forward voltage of the inverse diode $V_{SD}(t_h)$ are recorded.

By means of the calibration curve, the recorded values of $V_{SD}(0)$ and $V_{SD}(t_h)$ are converted to the corresponding values $T_c^*(0)$ and $T_c^*(t_h)$ respectively.

The channel-case transient thermal impedance for the heating pulse duration $t_h$ is calculated as:

$$Z_{thJC}(t_h) = \frac{[T_c^*(t_h) - T_c^*(0)] - [T_c(t_h) - T_c(0)]}{P(H) - P(M)}$$

(2)

where

$T_c^*(t_h)$, $T_c^*(0)$ are the values taken from the calibration curve for $V_{SD}(t_h)$ and $V_{SD}(0)$ respectively;

$T_c(t_h)$, $T_c(0)$ are the values at $t = t_h$ and $t = 0$ respectively;

$P(H) = I_D \cdot V_{DS}$ is the heating power in position 2;

$P(M) = I_M \cdot V_{SD}$ is the dissipation in position 1.

The channel-case thermal resistance $R_{thJC}$ is the value finally reached of $Z_{thJC}$ when the pulse duration is long enough to reach the new thermal equilibrium.
6.19 Verification of the forward-bias and reverse-bias safe operating area (FBSOA, RBSOA)

6.19.1 Verification of the forward-bias safe operating area (FBSOA)

6.19.1.1 Purpose

To verify the forward-bias safe operating area of a case-rated power field-effect transistor under specified conditions with non-inductive load.

6.19.1.2 Circuit diagram

![Circuit diagram](image)

Figure 28 – Circuit diagram

6.19.1.3 Circuit description and requirements

- \( V_{GG}, V_{DD} \) = adjustable voltage sources
- \( R_{G1}, R_{G2} \) = 10 kΩ or as specified
- \( R_s \) = non-inductive resistor for measuring \( I_D \)
- \( S \) = electromechanical or electronic switch to obtain the specified sequence of current pulse
- \( M_A, M_B \) = instrument (e.g. dual-beam oscilloscope) for measuring \( V_{DS} \) and \( I_D \).

6.19.1.4 Test procedure

The case temperature is set to the specified value.

With the switch operating with the specified pulse duration and duty cycle, \( V_{GG} \) and/or \( V_{DD} \) are increased until the specified pulse values for \( V_{DS} \) and \( I_D \) are reached.

Under these operating conditions, the device being measured is operated for the specified duration of the test, or for the specified number of pulses, as appropriate.

Verification of the FBSOA rating is obtained from the post-test measurements.

The device is considered defective if at any instant during the test the drain-source voltage collapses or oscillates during the fall of the current pulses.
6.19.1.5 Specified conditions
- Case temperature \( T_c \).
- Drain-source voltage \( V_{DS} \).
- Drain current \( I_D \).
- As specified, either d.c. operation or repetitive pulse operation, or a combination of these conditions.
- Pulse duration \( t_p \) and duty factor \( \delta \) as appropriate.
- As specified, either duration of the test or number of test pulses.
- \( R_{G1}, R_{G2} \) if other than 10 kΩ.
- Post-test measurement limits.

6.19.2 Verification of the reverse-bias safe operation area (RBSOA)

6.19.2.1 Purpose
To verify the reverse-bias safe operation area of a case-rated power field-effect transistor under specified conditions with inductive load.

6.19.2.2 Circuit diagram and test waveforms

\[ T = \text{transistor being measured (MOSFET or JFET)} \]

Figure 29 – Circuit diagram
6.19.2.3 Circuit description and requirements

D = clamping diode
L = inductive load
\( V_{GG1}, V_{GG2}, V_{DD} \) = adjustable voltage sources
\( V_{KK} \) = adjustable voltage source for the clamping voltage \( V_K \)
\( R_{G1}, R_{G2} \) = 10 k\( \Omega \) or as specified
\( R_S \) = non-inductive resistor for measuring \( I_D \)
S = electromechanical or electronic switch to obtain the specified sequence of current pulses
\( M_A, M_B \) = instrument (e.g. dual-beam oscilloscope) for measuring \( V_{DS} \) and \( I_D \)

6.19.2.4 Test procedure

The case temperature is set to the specified value.

With the switch opened, the clamping voltage \( V_K \) and the negative gate bias voltage \( V_{GG2} \) are set to their specified values.

With the switch operating with the specified pulse sequence (\( t_p \) and \( \delta \)), \( V_{GG1} \) and/or \( V_{DD} \) are increased until the peak value of the drain current and the drain-source voltage reach the specified values \( I_{DM} \) and \( V_{DS} \) respectively.

Under these operating conditions, the device under test is operated for the specified duration of the test, or for the specified number of pulses, as appropriate.
Verification of the RBSOA rating is obtained from the post-test measurements.

The device is considered defective if, at any instant during the test, the drain-source voltage collapses or oscillates during the fall of the current pulses.

6.19.2.5 Specified conditions
- Case temperature $T_c$.
- Drain-source voltage $V_{DS}$.
- Negative gate bias voltage $V_{GG2}$.
- Peak value of drain current $i_{DM}$.
- Clamping voltage $V_K$.
- Inductance $L$.
- As specified, either d.c. operation or repetitive pulse operation, or a combination of these conditions.
- Pulse duration $t_p$ and duty factor $\delta$ as appropriate.
- As specified, either duration of the test or number of test pulses.
- $R_{G1}, R_{G2}$ if other than 10 kΩ.
- Post-test measurement limits.

7 Acceptance and reliability

7.1 Electrical endurance tests

7.1.1 General requirements
Clause 2, chapter VII, section three, of IEC 60747-1, which has the same title, is valid.

7.1.2 Specific requirements

7.1.2.1 List of endurance tests
A choice of endurance tests is given in table 2, which are applicable for all subcategories of bipolar transistors.

7.1.2.2 Conditions for endurance tests
Test conditions and test circuits are listed in table 2. The relevant specification will state which test(s) will apply.

7.1.2.3 Failure-defining characteristics and failure criteria for acceptance tests
Failure-defining characteristics, their failure criteria and measurement conditions are listed in table 1.

NOTE Characteristics should be measured in the sequence in which they are listed in this table, because the changes of characteristics caused by some failure mechanisms may be wholly or partially masked by the influence of other measurements.

7.1.2.4 Failure-defining characteristics and failure criteria for reliability tests
Under consideration.
7.1.2.5 Procedure in case of a testing error

When a device has failed as a result of a testing error (such as a test equipment fault or measurement equipment fault, or an operator error), the failure shall be noted in a data record with an explanation of the cause.

Table 1 – Failure-defining characteristics for acceptance after endurance tests

<table>
<thead>
<tr>
<th>Acceptance criteria</th>
<th>Types A and B</th>
<th>Type C</th>
</tr>
</thead>
<tbody>
<tr>
<td>(0.8 \text{ LSL} &lt; V_{\text{GS off}} &lt; 1.2 \text{ USL})</td>
<td>(0.8 \text{ LSL} &lt; V_{\text{GS(TO)}} &lt; 1.2 \text{ USL})</td>
<td>(0.8 \text{ LSL} &lt; V_{\text{GS(TO)}} &lt; 1.2 \text{ USL})</td>
</tr>
<tr>
<td>Non-operatives</td>
<td>(V_{\text{GS off}} &gt; 3 \text{ } V_{\text{GS max.}})</td>
<td>(V_{\text{GS(TO)}} &lt; 0.1 \text{ } V_{\text{GS(TO) min.}})</td>
</tr>
<tr>
<td></td>
<td>(I_{\text{DS}} &lt; 10 \text{ } I_{\text{DS max.}})</td>
<td>(I_{\text{DS}} &gt; 10 \text{ } I_{\text{DS max.}})</td>
</tr>
</tbody>
</table>

**NOTE**

USL = upper specification limit
LSL = lower specification limit.

Table 2 – Conditions for the endurance tests

<table>
<thead>
<tr>
<th>Device categories</th>
<th>Tests</th>
<th>Operating conditions</th>
<th>Test circuits (note 2)</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power field-effect transistors for amplifier and switching applications</td>
<td>Operating life</td>
<td>(I_{0} = \frac{R_{ct \text{ max.}}}{V_{DS}})(^{(note 3)})</td>
<td>(V_{DD} = 2 \text{ } V_{DS})</td>
<td>(V_{DD} = 2 \text{ } V_{DS})</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(V_{DS} = 0.8 \text{ } V_{DS \text{ max.}})(^{(note 1)})</td>
<td></td>
<td>(R_{0} = \frac{V_{DS}}{I_{b}})</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(T_{\text{a} \text{ b}})</td>
<td></td>
<td>(R_{0} = 10 \text{ } k\Omega) preferably (note 5)</td>
</tr>
</tbody>
</table>

**NOTE 1** Test conditions shall be within the safe operating area if one is specified. The voltage is to be lowered below 0.7 \(V_{DS \text{ max.}}\) only as much as necessary to remain within the safe operating area.

**NOTE 2** Change circuit appropriately for other types of FETs than n-channel enhancement type.

**NOTE 3** See subclause 2.1.5, chapter VIII, section three, of IEC 80747-1.

**NOTE 4** See subclause 2.1.3, chapter VIII, section three, of IEC 60141-1.

**NOTE 5** In order not to exceed \(V_{DS \text{ max.}}\), a clamping circuit may be added to limit \(V_{GS\text{.}}\)
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